IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

LIONRA TECHNOLOGIES LTD. v. CISCO SYSTEMS, INC.	Case No. 2:24-cv-00097-JRG **JURY TRIAL DEMANDED**

DEFENDANT CISCO SYSTEMS, INC.'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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Cisco requests construction of only two terms in the patent-in-suit. Both terms require a straightforward application of the intrinsic record and applicable law to arrive at the correct construction.

First, Cisco seeks to construe the phrase "concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory" to require that the term "concurrently" applies to both numbered items. Specifically, Cisco seeks a ruling that "each individual one of said plurality of headers" must be written to each respective protocol stack layer memory concurrently.

Middle-school grammar rules dictate that a modifier before a numbered list modifies each item in the list. Here, the modifier "concurrently writing" modifies both (1) a plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory. And therefore, the claims require that the plurality of headers be written concurrently to each of the respective protocol stack layer memories. This plain-language interpretation is also consistent with each of the embodiments described in the specification, and is required to enable the recited benefits.

Even if it weren't crystal clear from the claim language and specification, Cisco's proposed construction is further supported by a clear and unmistakable prosecution history disclaimer. To distinguish the claimed invention, the applicant stated that the allegedly anticipatory prior art is "entirely different" than the claimed invention because the prior art does not teach that "***each individual one of a plurality of headers in a packet are written concurrently to a respective protocol stack layer memory location***." Ex. 1 (Reply to Office Action of Dec. 21, 2009) at 4 (emphasis added). The claims were allowed without amendment shortly after applicant made this disclaimer. Thus, the intrinsic evidence mandates Cisco's construction.

Second, Cisco requests that the Court apply the patent's explicit definition of the claim term "packet buffer memory." The patent plainly defines the term: "***The CPU main memory space used for the packet transfer is known as the packet buffer memory 122***." '471 Patent at 5:49-51 (emphasis added). The specification is also unequivocal that packet buffer memory 122 is the packet buffer memory of the claims. For example, packet buffer memory 122 is identified in both figures depicting the preferred embodiments of the claims. Packet buffer memory 122 is also identified more than a dozen times in the specification describing the claimed invention. The Federal Circuit and this Court have consistently held that a patentee's lexicography governs, as it should here.

Since the intrinsic record mandates both of Cisco's proposed constructions and both are essential to clarify the proper scope of the claims for the jury, Cisco respectfully requests that this Court adopt Cisco's constructions.

I. OVERVIEW OF THE '471 PATENT

U.S. Patent No. 7,738,471 ("the '471 Patent") is directed to processing packets of data in wireless networks. '471 Patent at Abstract, 1:6-11. Devices, or nodes, in a wireless network communicate with each other using data formats called protocols. *Id.* at 1:13-29. Two of the most common protocols are internet protocol (IP) and transmission control protocol/internet protocol (TCP/IP). *Id.* Under these protocols, each packet has a plurality of headers which contain the fields that each device processes to transmit the packet. *Id.* at 1:40-61. Some of these headers "have long fields that require a comparison among several values," meaning "packet transmission often experiences relatively long delays due to protocol header processing." *Id.* at 1:59-65.

Although "[m]any solutions [had] been proposed for decreasing the protocol header processing time," *id.* at 1:66-67, the '471 Patent focuses on the shortcomings of the "sequential processing approach" *id.* at 2:2-44. Sequential processing "involves receiving an encoded packet at a node, decoding the received encoded packet, and processing protocol headers of the decoded packet in a *sequential* manner." *Id.* at 2:2-6 (emphasis added). Notably, "the sequential processing approach is dependent on methods to advance the protocol header processing from one protocol header to a next protocol header." *Id.* at 2:6-9.

An example of the prior art sequential process is illustrated in FIG. 5:

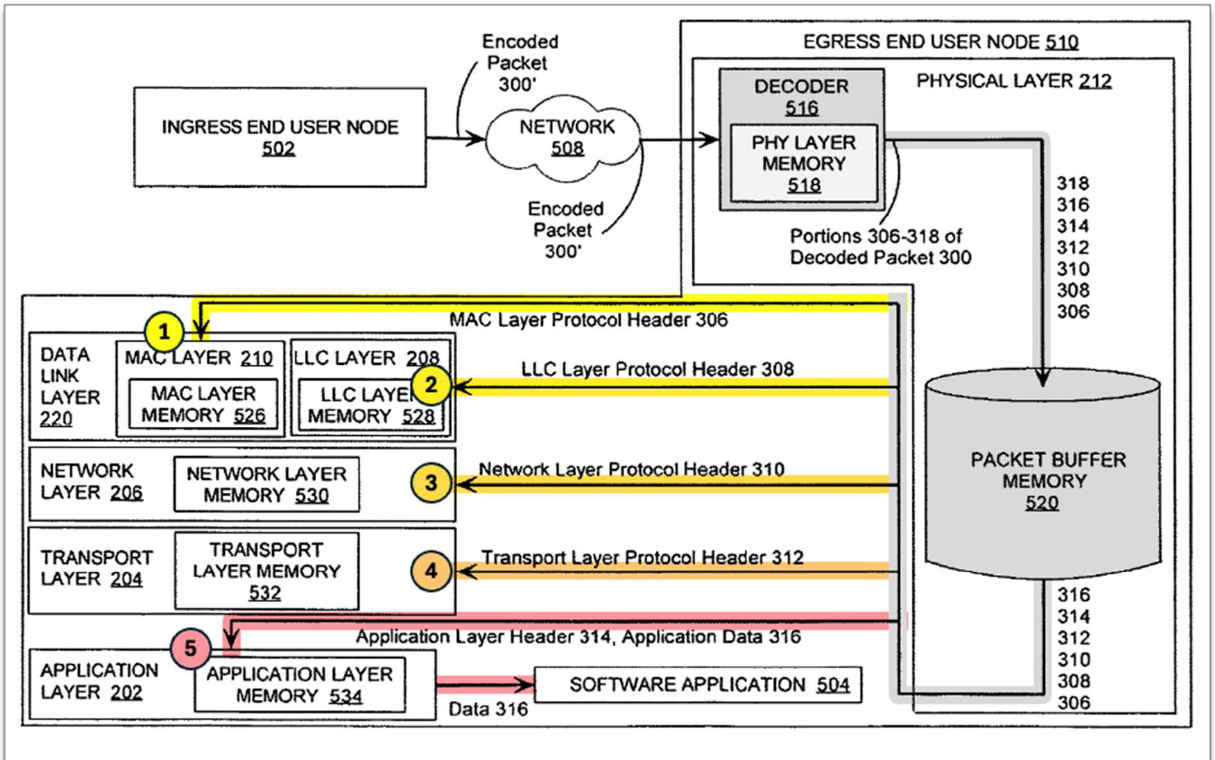


FIG. 5
(PRIOR ART)

Id. at FIG. 5 (annotated).

According to the patent, a major drawback of the sequential approach is the amount of time it takes to complete processing of all headers in a sequential manner. *See, e.g.*, '471 Patent at 2:57-59. More specifically, the disclosed sequential processing approach involves receiving a packet, decoding it, processing the preamble of the packet, writing each protocol stack layer header to a packet buffer memory for storage, and then each layer accessing the packet buffer memory to retrieve and process each layer header one at a time. *See id.* at 2:14-44, 10:47-48.

So, for example, as depicted above, after the packet is received, decoded, and written to memory, the decoder (516) first notifies the media access control (MAC) layer (210) that the MAC layer protocol header (306) is stored in the packet buffer memory (520). '471 Patent at 10:47-63. Then the MAC layer retrieves the MAC layer protocol header from the packet buffer memory and stores it in the MAC layer memory (526). *Id.* After the MAC layer completes the relevant processing, it then notifies the logic link control (LLC) layer (208) that it is the LLC layer's turn to retrieve and process the LLC layer protocol header (308). *Id.* The LLC layer then retrieves and stores the LLC layer protocol header in the LLC layer memory (528) and performs the relevant processing. *Id.* at 10:64-11:7. After the LLC layer has completed that process, the LLC layer notifies the network layer (206). *Id.* This process is repeated sequentially until the processing of each layer protocol header is complete. *Id.* at 11:3-16.

In an attempt to "reduce protocol header processing time," the '471 Patent discloses using a DMA device "to concurrently write the specific layer header fields directly into: (a) each protocol stack layer's internal memory spaces 126, . . . ; and (b) the packet buffer memory 122." '471 Patent at 5:64-6:6. Packet buffer memory 122 is the "CPU main memory space used for the packet transfer." *Id.* at 5:49-51. By having the headers written to the main memory of the CPU concurrently with each individual protocol stack layer memory, the patent purports to "reduce[] processing latency" and "increase[] bandwidth." *Id.* at 6:28-31. This benefit is only possible because "the DMA device (120) is configured to allow each of the protocol stack layers to ***concurrently begin*** header processing." *Id.* at 6:24-28 (emphasis added). "For example, respective headers of a packet are ***concurrently processed*** in the MAC layer, the LLC layer, the network layer, the transport layer and the application layer." *Id.* at 6:28-31 (emphasis added).

Thus, there are two major differences in the claimed system depicted in FIG. 4 when compared to prior art FIG. 5. First, FIG. 4 includes a DMA Device 120—a dedicated integrated circuit for transferring data to and from the CPU main memory without requiring the CPU to perform the read and write functions. '471 Patent at FIG. 4, 5:30-36. And second, as displayed below, the DMA device concurrently writes the headers to the packet buffer memory and the respective protocol stack layer memories. *Id.* at 9:41-10:5.

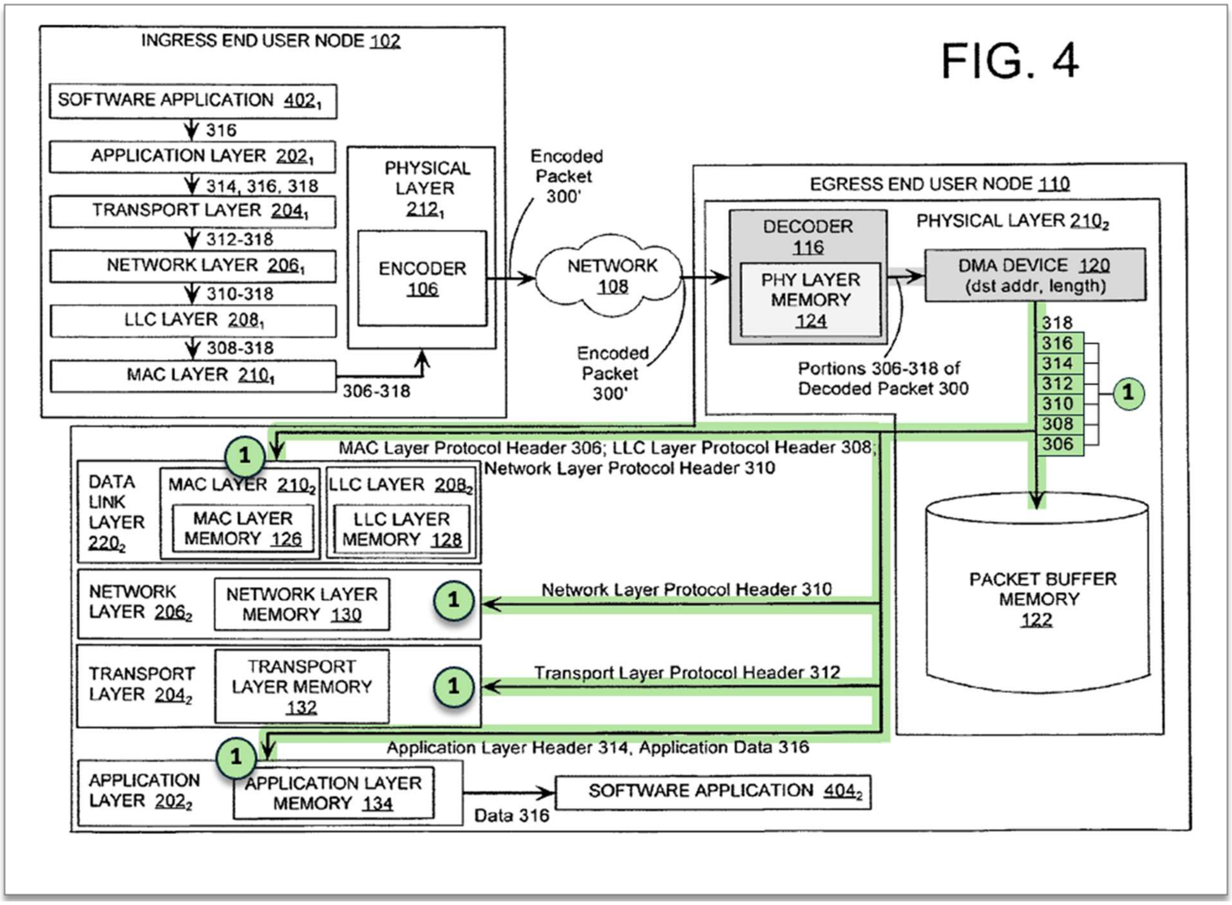


FIG. 4

Id. at FIG. 4 (annotated).

More specifically, the DMA device is "configured to concurrently communicate data to the packet buffer memory 122, the media access control (MAC) layer memory 126, the logic link control (LLC) layer memory 128, the network layer memory 130, the transport layer memory 132, and the application layer memory 134." '471 Patent at 6:14-19. Writing "to these various memory locations in a single DMA transaction" enables "each of the protocol stack layers to concurrently begin header processing without having to wait for one or more other protocol stack layers to complete its header processing." *Id.* at 6:20-21, 6:26-28. In other words, concurrently writing each of the respective headers of a packet in each respective memory enables them to be "concurrently processed in the MAC layer, the LLC layer, the network layer, the transport layer and the application layer." *Id.* 6:28-31.

II. DISPUTED TERMS IN THE '471 PATENT

A. "concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory" (claims 1, 13)

Cisco's Proposal	Lionra's Proposal
Plain meaning, i.e., "concurrently writing (1) each of said plurality of headers to a CPU main memory space used for the packet transfer and (2) each individual one of said plurality of headers (each concurrently with each other) to a respective protocol stack layer memory."	No construction necessary. Plain and ordinary meaning.

1. The plain English words of the claim mandate Cisco's proposed construction, especially in view of the specification

Cisco seeks to construe the phrase "concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory" to require that the term "concurrently" applies to both numbered items. Specifically, Cisco seeks a ruling that "each individual one of said plurality of headers" must be written to each respective protocol stack layer memory concurrently. In contrast, Lionra contends that this language only requires concurrently writing a single header to the packet buffer memory and a single respective protocol stack layer memory.

The Court need look no further than the plain English language of the claims to resolve this dispute. As is readily apparent, the modifier "concurrently writing" applies to both items in the numbered list. As the Federal Circuit has recognized, it is a "general grammatical principle" that a modifier that comes before a series modifies each item in the series. *SIMO Holdings Inc. v. Hong Kong uCloudlink Network Tech. Ltd.*, 983 F.3d 1367, 1377 (Fed. Cir. 2021) (citing Antonin Scalia & Bryan A. Garner, *Reading Law: The Interpretation of Legal Texts* § 19, 147 (2012)). "Th[is] principle has particular force when [like here] the term joining the items in a series is 'and.'" *Id.* (citing *SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 886 (Fed. Cir. 2004)). Thus, a straightforward application of this general grammatical principle dictates that "concurrently writing" also modifies the phrase "each individual one of said plurality of headers to a respective protocol stack layer memory." In other words, the plain and ordinary meaning requires that the headers must be written each concurrently with each other to their respective protocol stack layer memories.

The specification confirms this reading. For example, the specification explains that the DMA device is "configured to ***concurrently communicate data*** to the packet buffer memory 122, the media access control (MAC) layer memory 126, the logic link control (LLC) layer memory 128, the network layer memory 130, the transport layer memory 132, ***and*** the application layer memory 134." '471 Patent 6:14-19 (emphases added). And further, the "DMA device is used to ***concurrently write*** the specific layer header fields directly into: (a) ***each*** protocol stack layer's internal memory spaces 126, . . . , 134 to initiate immediate processing." *Id.* at 5:58-6:6 (emphases added).

This concurrent writing of the each of the headers to the respective memories is also necessary to enable to claimed benefits. For example, writing "to these various memory locations in a single DMA transaction" enables "each of the protocol stack layers to concurrently begin header processing." *Id.* at 6:20-21, 6:26-28. In other words, concurrently writing each of the headers of a packet to the respective protocol stack layer memories enables them to be "concurrently processed in the MAC layer, the LLC layer, the network layer, the transport layer and the application layer." *Id.* 6:28-31. Thus, concurrently writing each of the headers to each protocol stack layer memory enables concurrent header processing to "provide[] an increased packet processing time," a key alleged benefit of the invention. *Id.* at 10:12-16. Cisco's proposed construction enables this benefit, whereas no such benefit would be gained under Lionra's stated interpretation.

In other words, under the plain meaning of the claims in view of the specification, the phrase "concurrently writing" modifies both (1) writing a plurality of headers to a packet buffer memory and (2) writing each individual one of said plurality of headers to a respective protocol stack layer memory. Cisco's proposed construction gives effect to the plain meaning of the claim language as confirmed by the specification.

2. The prosecution history further confirms Cisco's proposed construction is correct

If there were any doubt about the meaning of the disputed phrase from its plain language—and there should be none—the prosecution history erases that doubt. During prosecution of the '471 Patent, the applicant distinguished the claimed invention from an allegedly anticipatory prior art reference, U.S. Pub. No. 2001/0037397 ("Boucher"), by stating that Boucher "is entirely different from the system recited in Applicant's claim 1, where ***each individual one of a plurality of headers in a packet are written concurrently to a <u>respective</u> protocol stack layer memory location***." Ex. 1 (Reply to Office Action of Dec. 21, 2009) at 4 (bold and italics added, underlining in original). As the applicant further explained, "Boucher does not teach the step of ***concurrently***

writing 'each individual one of said plurality of headers to a respective protocol stack layer memory where it is available for immediate processing within a protocol stack layer.'" *Id.* at 3 (emphasis added). This distinction is critical because Boucher is "a conventional arrangement in which processing proceeds sequentially from one layer to the next." *Id.* at 4.

In other words, the applicant unequivocally explained that the claimed invention requires both: (1) concurrently writing each header to a packet buffer memory and (2) ***concurrently writing each individual one of said plurality of headers to a respective protocol stack layer memory***. *Id.* at 3-4. The claims were allowed without amendment after the applicant made this disclaimer. Ex. 2 (Notice of Allowance).

This Court and other courts in this District have found prosecution history disclaimer under similar circumstances. *See, e.g.*, *United Servs. Auto. Ass'n v. Truist Bank*, No. 2:22-CV-00291-JRG-RSP, Dkt. 186 at 43 (E.D. Tex. Sept. 27, 2023) (finding prosecution history disclaimer when a patentee explicitly distinguished the claimed invention over a prior art reference by stating that the claimed invention required a feature not disclosed by the prior art); *Huawei Techs. Co. v. T-Mobile US, Inc.*, No. 2:16-CV-00052-JRG-RSP, 2017 WL 4385567, at *1-3 (E.D. Tex. Sept. 9, 2017), *report and recommendation adopted*, No. 2:16-CV-00052-JRG-RSP, 2017 WL 4310161 (E.D. Tex. Sept. 28, 2017) (finding disclaimer of certain techniques when patent owner in an IPR affirmatively stated that challenged claims required the techniques, and that the prior art lacked them); *see also R2 Sols. LLC v. Databricks, Inc.*, No. 4:23-CV-1147, 2024 WL 5058965, at *2 (E.D. Tex. Dec. 10, 2024) ("[B]y distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover.") (quoting *Spectrum Int'l v. Sterilite Corp.*, 164 F.3d 1372, 1378-79 (Fed. Cir. 1988)).

Since the prosecution history unequivocally mandates Cisco's proposed construction—which is consistent with the plain language of the claims and the patent specification—the Court should adopt Cisco's proposal.

3. Lionra's arguments mischaracterize and are inconsistent with the intrinsic record

Lionra's proposed interpretation conflicts with the prosecution history, the plain language of the claims, and large swaths of the specification—some of which Lionra itself cites. For example, Lionra states that the claims recite "concurrently writing" to (1) "a packet buffer memory" and (2) "a respective protocol stack layer memory." Dkt. 35 at 1. But this framing excludes key claim language, essentially reinterpreting the claim language as follows: "concurrently writing (1) ~~each of said plurality of headers~~ to a packet buffer memory and (2) ~~each individual one of said plurality of headers~~ to a respective protocol stack layer memory."

Otherwise stated, Lionra incorrectly interprets the claim language to mean that the concurrent writing step is satisfied so long as the DMA device concurrently writes a single header to a packet buffer memory and to a *single* respective protocol stack layer memory. Dkt. 35 at 1-3. But the claims are not so broad. Lionra should not be permitted to ignore the "each individual one of said plurality of headers" language stated in the claim.

Further, despite Lionra's mischaracterizations, none of the other support cited by Lionra is inconsistent with Cisco's proposed construction. For example, Lionra relies on the "preferred embodiment described in Figure 4," arguing that it involves "separate write operations" for each header and "does not describe a 'concurrent' write with respect to the MAC layer memory and the LLC layer memory." Dkt. 35 at 3. But Lionra proceeds to block-quote an excerpt describing this embodiment which says the exact opposite. Dkt. 35 at 3-4; '471 Patent at 9:41-10:5 ("More specifically, the DMA device 120 ***concurrently performs a plurality of write operations***. The write operations include a write operation for concurrently communicating the media access control (MAC) layer protocol header 306 to the packet buffer memory 122 and the media access control (MAC) layer memory 126. The ***write operations also include*** a write operation for concurrently communicating the logic link control (LLC) layer protocol header 308 to the packet buffer memory 122 and the logic link control (LLC) layer memory 128 . . ***and so on***.") (emphases added). In other words, Cisco agrees with Lionra that concurrently writing each header to a packet buffer memory and a respective protocol stack layer memory involves separate write operations. But, as explained by the specification excerpt that Lionra cites, ***each*** of the write operations to the respective protocol stack layer memories must also be performed ***concurrently***. *Id.*

For further example, Lionra also cites an embodiment in which the DMA device "concurrently write[s] the headers and payload to the packet buffer memory 122 and at least one of the MAC layer memory 128**,** the network layer memory 126, the LLC layer memory 130, the transport layer memory 132, and the application layer memory 134." Dkt. 35 at 3 (quoting '471 Patent at 6:38-44). Lionra uses the "at least one of" language in this excerpt to contend that the claims only require writing to a packet buffer memory and a ***single*** respective protocol stack layer. *Id.* at 3-5. But this interpretation is incorrect in view of the plain language of the claims (as discussed above), as well as common claim construction principles. For example, in *SuperGuide*, the Federal Circuit held that the plain meaning of "at least one of" when preceding a list that includes the conjunctive "and" means at least one of each item in the list. So, for example, if a patent says, "at least one of" A, B, and C, it presumptively means: at least one A, at least one B, and at least one C. *SuperGuide*, 358 F.3d at 886. Similarly, here, the cited excerpt says, "***at least one of*** the MAC layer memory 128**,** the network layer memory 126, the LLC layer memory 130, the transport layer memory 132, ***<u>and</u>*** the application layer memory 134." '471 Patent at

6:38-44 (emphases added). Therefore, consistent with Cisco's construction, and directly contrary to Lionra's interpretation, this excerpt means that the DMA concurrently writes to ***at least one*** MAC layer memory 128, ***at least one*** network layer memory 126, ***at least one*** the LLC layer memory 130, ***at least one*** transport layer memory 132, <u>***and***</u> ***at least one*** application layer memory 134.

Similarly, Lionra cites several other excerpts from the specification to argue that Cisco's construction would "exclude" them. Dkt. 35 at 2-3. Yet none of these excerpts are inconsistent with Cisco's construction, as each citation merely echoes the claim language. Otherwise stated, Lionra's arguments that Cisco's proposed construction is inconsistent with these excerpts rests on Lionra's misinterpretation of the claim language as requiring concurrent writing to ***only*** (1) the packet buffer memory and (2) ***a single*** respective protocol stack layer memory. *Id.* (citing'471 Patent at 3:11-15, 3:49-54, 5:64-6:1, 6:38-44).

* * *

In sum, the Court should adopt Cisco's construction for three reasons. First, because the plain English language of the claims require that "concurrently writing" applies to both numbered items in the list. Second, because the specification supports this understanding. And third, because the applicant made a clear and unmistakable disclaimer during prosecution mandating Cisco's construction. As such, the Court should construe the term "concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory" to mean "concurrently writing (1) each of said plurality of headers to a CPU main memory space used for the packet transfer and (2) each individual one of said plurality of headers (<u>each concurrently with each other</u>) to a respective protocol stack layer memory."

B. "packet buffer memory" (claims 1, 13)

Cisco's Proposal	Lionra's Proposal
"CPU main memory space used for the packet transfer"	No construction necessary. Plain and ordinary meaning.

The '471 Patent **defines** "packet buffer memory" as the "CPU main memory space used for the packet transfer." '471 Patent at 5:49-51. Cisco seeks only to enforce that explicit definition. Lionra's reliance on extrinsic evidence to attempt to avoid this clear lexicography only demonstrates why a jury would benefit from Cisco's construction, which clarifies the meaning of the term in the context of the '471 Patent.

As the Federal Circuit has held, "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess." *AIA Eng'g Ltd. v. Magotteaux Int'l S/A*, 657 F.3d 1264, 1276 (Fed. Cir. 2011) (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314-17 (Fed. Cir. 2005) (en banc)). "In such cases, the inventor's lexicography governs." *Id.* (cleaned up). Here, the specification provides a clear lexicography for the claim term "packet buffer memory": ***"The CPU main memory space used for the packet transfer is known as the packet buffer memory 122."*** '471 Patent at 5:49-51 (emphasis added).

Courts in this District and others have found the phrase "known as" to constitute definitional language. *See EpicRealm, Licensing, LLC v. Autoflex Leasing, Inc*, No. 2:05-CV-163, 2006 WL 3099603, at *10 (E.D. Tex. Oct. 30, 2006) ("The specification ***defines*** HTTP as 'a communications protocol ***known as*** HyperText Transport Protocol (HTTP).' . . . [T]he Court adopts a construction of 'HTTP-compliant device' to mean 'a device that is compliant with the communication protocol known as HyperText Transport Protocol (HTTP).'") (emphases added); *GlaxoSmithKline LLC v. Anchen Pharms., Inc.*, No. CA 11-046-RGA, 2012 WL 5594540, at *3

(D. Del. Nov. 15, 2012) ("The ***'known as'*** language also makes clear that 'solvates' was intended to be ***defined*** by the preceding description of complexes.") (emphases added); *Dali Wireless, Inc. v. Corning Optical Commc'ns LLC*, No. 20-CV-06469-EMC, 2021 WL 3037700, at *10 (N.D. Cal. July 19, 2021) ("[T]he specification expressly ***defines*** what sectors are. The specification states at one point: 'A typical base station comprises 3 *independent radio resources, commonly* ***known as*** sectors.'") (bold added, italics in original).

The specification also makes clear elsewhere that the defined "packet buffer memory 122" is the "packet buffer memory" of the claims. For example, the Abstract uses "a packet buffer memory (122)" interchangeably with "the packet buffer memory" in describing the claimed invention. *Id.* at Abstract ("The concurrent writing step involves concurrently writing each of the headers (306-314) to ***a packet buffer memory (122)*** . . . . More specifically, a MAC layer protocol header (306) is concurrently written to ***the packet buffer memory*** . . ."). The specification also cites this component when explaining the Patent's alleged novelty over the prior art. *Id.* at 5:64-6:1 ("In order to solve this problem, a DMA device is used to concurrently write the specific layer header fields directly into: . . . ***the packet buffer memory 122***."). And "packet buffer memory 122" appears in the only two figures that show block diagrams of the invention: FIG. 1, which depicts "a packet-based communications system that is useful for understanding the present invention," and FIG. 4, which is "a more detailed block diagram of the packet-based communication system in FIG. 1." *Id.* at 4:20-22, 4:28-29. In other words, "packet buffer memory 122" is the "packet buffer memory" in the embodiments of the asserted claims.

Attempting to avoid this definitional statement, Lionra argues that Cisco's construction comes from "a prior art embodiment." Dkt. 35 at 6. But Lionra is incorrect. Cisco's construction is simply the patentee's stated definition of "packet buffer memory 122," which is used to describe the claimed packet buffer memory throughout the Patent.[1] '471 Patent at 5:49-51. And, while the specification is discussing "conventional" architectures in the sentences surrounding the clear definition for this claim term, it only does so to explain the problem solved by the patent. *See, e.g.*, *id.* at 5:64-6:1 ("DMA devices [in conventional architectures] are provided only for a one time transfer of a packet from the MAC layer memory to a CPU main memory. In order to solve this problem, a DMA device is used to concurrently write the specific layer header fields directly into: . . . ***the packet buffer memory 122***.").

Nowhere is "packet buffer memory 122" included in a prior art embodiment. In fact, packet buffer memory 122 is included in all the preferred embodiments of the claimed invention. *See, e.g.*, *id.* at FIG. 1, FIG. 4.

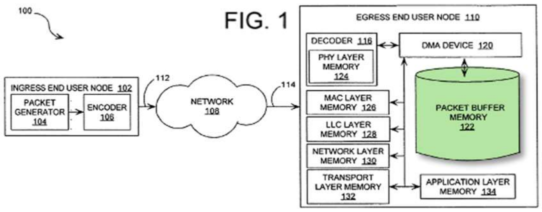


FIG. 1

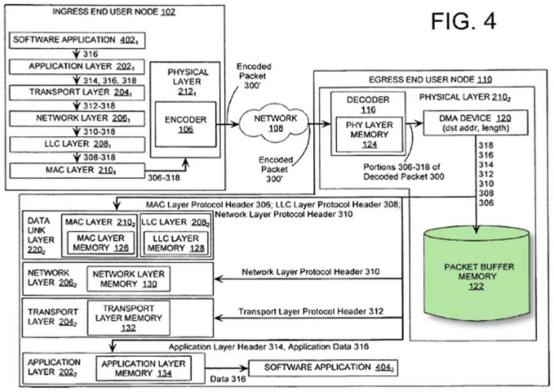
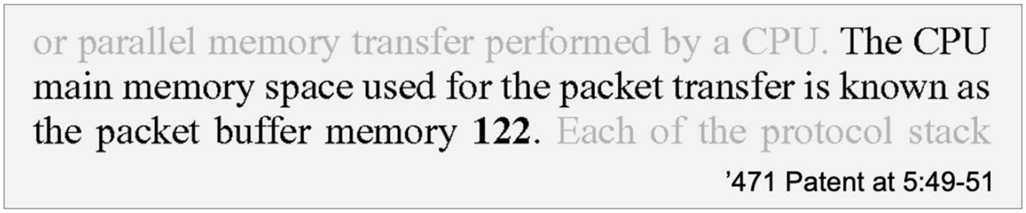


FIG. 4


or parallel memory transfer performed by a CPU. The CPU main memory space used for the packet transfer is known as the packet buffer memory **122**. Each of the protocol stack

'471 Patent at 5:49-51

[1] Notably, Lionra cites the term "packet buffer memory 122" ***nine*** times in specification excerpts while arguing for its construction of "concurrently writing (1) each of said plurality of headers to a packet buffer memory and (2) each individual one of said plurality of headers to a respective protocol stack layer memory." Dkt. 35 at 1-5. Presumably, Lionra does not believe that each of these excerpts is describing a prior art embodiment.

Lionra is also incorrect that "Cisco's construction would improperly exclude the preferred embodiments." Dkt. 35 at 6. Lionra's basis for this argument appears to be that "[t]he preferred embodiments of the invention do not include a CPU." *Id.* But while the figures do not depict a CPU, it is undisputed that the preferred embodiments ***do*** include "packet buffer memory 122," which the patent defines as "[t]he CPU main memory space used for the packet transfer." '471 Patent at 5:49-51; Dkt. 35 at 7. And it would make little sense to include an entirely separate depiction of a CPU in these embodiments when the embodiments already include a component which is, by definition, the CPU main memory space. It makes even less sense to argue that Cisco's construction excludes an embodiment that includes packet buffer memory 122, as Cisco is merely attempting to account for the definition of this very component put forward by the patent drafter.

Finally, Lionra's extrinsic evidence is irrelevant because the patentee's lexicography governs. *See C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 863 (Fed. Cir. 2004) (finding that "dictionary definitions are largely unhelpful" because "the ordinary and customary meaning of a term does not govern if the intrinsic record contains clear lexicography or disavowal of claim scope."). As such, Lionra's citations to expert testimony, a dictionary definition, and two unrelated patents to argue that "the plain and ordinary meaning of 'packet buffer memory' should not be limited to only 'CPU main memory space'" are unpersuasive and irrelevant. Dkt. 35 at 9. In other words, even if "packet buffer memory" can have other meanings in other contexts, that does not change the clear lexicography provided by the '471 Patent in this context: "***The CPU main memory space used for the packet transfer is known as the packet buffer memory 122***." '471 Patent at 5:49-51. Accordingly, the Court should adopt Cisco's construction which reflects this lexicography.

III. CONCLUSION

For the foregoing reasons, Cisco's proposed constructions of the two terms in dispute should be adopted.

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on March 19, 2025, the foregoing was electronically filed with the Clerk of the Court using the CM/ECF system, which will send a notice of electronic filing to CM/ECF participants in this case.

/s/ Brian A. Rosenthal
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